VP113
CLAIMS:

1. A method for burst mode data transfers between a CPU and a FIFO, the CPU adapted to execute a burst mode memory access instruction defining multiple memory addresses, the method comprising the steps of:

decoding the multiple memory addresses to produce an output that is the same for each of the multiple memory addresses; and

accessing the FIFO repeatedly, for each of the multiple addresses, by use of said output.

2. The method of claim 1, the method further comprising placing the multiple memory addresses sequentially on a bus, and sequentially receiving the multiple memory addresses from the bus for said step of decoding.

3. The method of claim 1, wherein said step of accessing is read accessing.

4. The method of claim 1, wherein said step of accessing is write accessing.

5. An apparatus for burst mode data transfers by a CPU, the CPU adapted to

execute a burst mode memory access instruction defining multiple memory addresses, comprising:

a FIFO; and

a decoder, said decoder adapted for receiving and decoding the multiple memory addresses so as to produce an output that is the same for each of said multiple memory addresses, and providing said output to said FIFO for accessing said FIFO.

6. The apparatus of claim 5, wherein the CPU and said decoder are coupled to a bus, wherein said decoder is adapted to sequentially receive the multiple memory addresses from the bus.

7. The apparatus of claim 5, wherein said output of said decoder is for read accessing said FIFO.

8. The apparatus of claim 5, wherein said output of said decoder is for write accessing said FIFO.

9. A medium readable by a machine embodying a program of instructions executable by the machine to perform a method for burst mode data transfers between a CPU

and a FIFO, the CPU adapted to execute a burst mode memory access instruction defining multiple memory addresses, the method comprising the steps of:

decoding the multiple memory addresses to produce an output that is the same for each of the multiple memory addresses; and

accessing the FIFO repeatedly, for each of the multiple addresses, by use of said output.

10. The medium of claim 9, wherein the method further comprises placing the multiple memory addresses sequentially on a bus, and sequentially receiving the multiple memory addresses from the bus for said step of decoding.

11. The medium of claim 9, wherein the method further comprises read accessing the FIFO.

12. The medium of claim 9, wherein the method further comprises write accessing the FIFO.

13. A system for burst mode data transfers, comprising:

a CPU adapted to execute a burst mode memory access instruction

defining multiple memory addresses;

a FIFO; and

a decoder, said decoder adapted for receiving and decoding the multiple memory addresses so as to produce an output that is the same for each of said multiple memory addresses, and providing said output to said FIFO for accessing said FIFO.

14. The system of claim 13, further comprising a bus, wherein said CPU and said decoder are coupled to said bus, wherein said decoder is adapted to sequentially receive the multiple memory addresses from said bus.

15. The system of claim 13, wherein said output of said decoder is for read accessing said FIFO.

16. The system of claim 13, wherein said output of said decoder is for write accessing said FIFO.